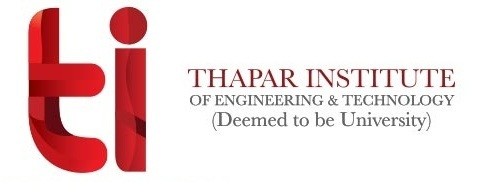
**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**



Analog IC Design

**Experiment-7**

**Submitted by**

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**M.Tech (VLSI Design)**

**Experiment-7**

**Aim**:

To design a differential amplifier with active load for a gain 100 and analyse its transient characteristics.

**Tool Used:**

LTspice tool

**Theory:**

Differential amplifiers amplify the difference between two voltages making this type of operational amplifier circuit a Subtractor unlike a summing amplifier which adds or sums together the input voltages.

For a Level NMOS let’s assume

VDD = 1.8V

VT = 0.4V

Kn = 120µA/V2,

For a Level PMOS let’s assume

VDD = 1.8V

VT = -0.4V

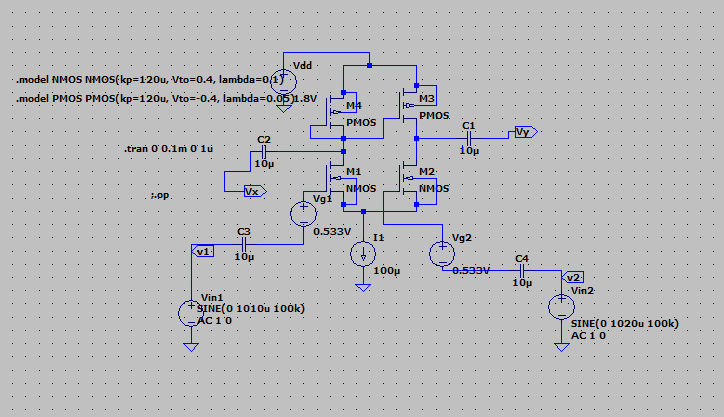
Kp = 120µA/V2,

Which gives a value of (W/L) = (46.8) for 1mA ID.

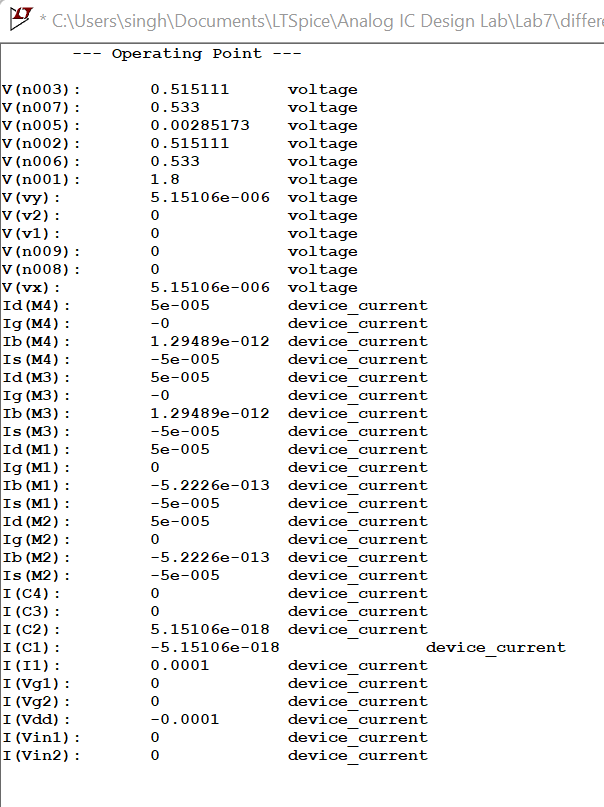
The value of VDS should be maintained above (VGS - VT = 0.6 - 0.4 = 0.2V) for the transistor to stay in saturation region.

As for M2 and M1, the width is taken as 468 µm and the length is taken as 10µm and for M3 and M4, the width is taken as 10 µm and the length is taken as 10 µm.

**Circuit Schematic:**

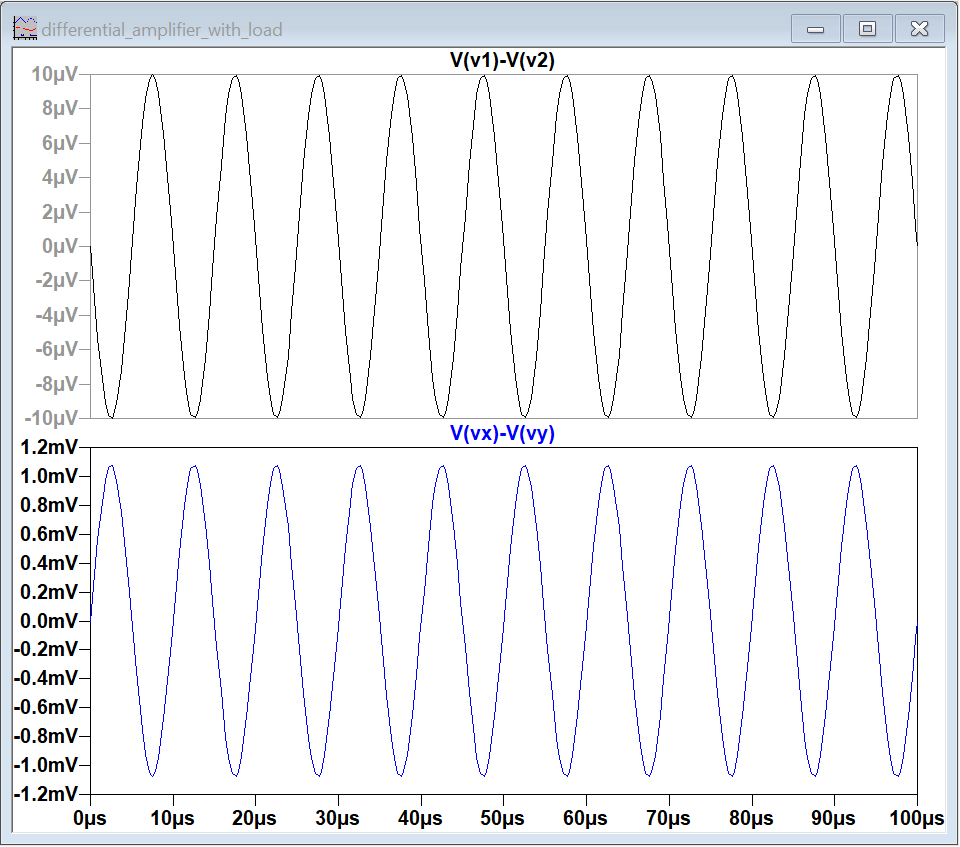
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**DC Operating Point**

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**Output Waveforms:**

Transient Response:



Resu**lt:**

The circuit is designed for a gain of 100 and the output is verified to be correct.